IDR RID Report

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Section 3.4.1 **Page** 3-41 to 3-45 **Figure Table** Fig. 3.4.1-1,

Category Name ISS Design **Actionee** ECS
Sub Category
Subject Matching LAN Design to Data Flow Requirements

Description of Problem or Suggestion:

The level of detail of both the table and figure make it difficult to assess whether the LAN design meets the data flow requirements. For instance the table lists Data Server to Processing, but not a corresponding "from", whereas other rows in the same table indicate "to/from". Does this row include both to/from? This is compounded with the lack of rates LAN diagram for various paths, and the fact that the diagram shows two DS Hosts with HiPPI interface. Is this both FSMS hosts or an APC and FSMS host?

Originator's Recommendation

Break up the flows in Table 3.4.1.1-1 into "to" and "from" to make correlation with the technical baseline easier. On the LAN diagram, show the expected data flow rates for each path, alongside the rates provided by the LAN design.

GSFC Response by: **GSFC Response Date**

HAIS Response by: E. Jalleta **HAIS Schedule** 12/3/95
HAIS R. E. M. Armstrong **HAIS Response Date** 12/14/95

Because the DAAC hardware and network design is at an IDR level, the exact number and configuration of hosts and networks have not been defined. This level of definition will be performed for CDR in April 1996.

For IDR, the network flows presented in the 305 tables reflect aggregate flows between subsystems. For instance, one column shows the total flows between Processing and Data Server (note that all columns should refer to "to/from" flows; the "to" flow is mislabeled). Since the exact number of processing and data server hosts are not finalized, it is impossible at this stage to determine the exact network traffic at a host level. The figures presented for IDR are meant to show that the proper classes of technology are in place to handle expected loads. For instance, some DAACs have very high network rates and therefore have been designed with an 800 Mbps HiPPI network. This network connects the Processing and DS hosts together, but at this time we can not say exactly how many hosts will be connected or how many interfaces on the HiPPI switch will be required. The same applies for the FDDI network: the figures reflect that FDDI will support the range of flows indicated in the sizing tables. The figures show that some hosts, if necessary, can have their own dedicated 100 Mbps FDDI interface, while other hosts requiring less bandwidth can share a single FDDI interface. This level of design detail will be part of the CDR design, for which a more detailed analysis will be provided, showing that the network design (a host design) supports the required data rates.

Thus, in summary, the IDR level of design shows the classes of technology and general topologies available to satisfy data flow requirements. The detailed design showing exact host connections and exact data flows on a host level will be presented for CDR.

Status **Closed** **Date Closed** **1/25/96** **Sponsor** **desJardins**

****** **Attachment if any** ******